UNLEASH NEXT-LEVEL SCALAR COMPUTE

AMD
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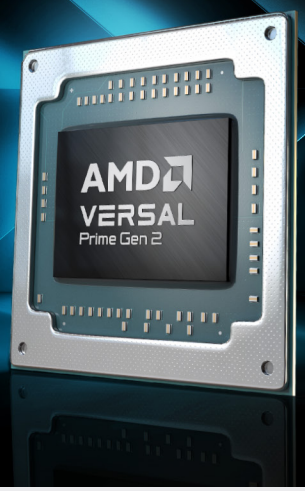

OVERVIEW

AMD Versal™ Prime Series Gen 2 adaptive SoCs combine world-class programmable logic from AMD with a new high-performance processing system of integrated Arm® CPUs—offering up to 10X more scalar compute than existing Versal or Zynq™ adaptive SoCs.[1] This powerful combination of flexible, real-time sensor processing and the ability to handle complex embedded computing workloads allows designers to maximize system performance while avoiding the overhead of a multi-chip solution.

Designed for a broad range of applications including 8K video processing, avionics, and more, the Versal Prime Series Gen 2 devices offer expanded hardened IP to complement the programable logic and processing system. This new IP includes hardened video encode & decode,[2] DDR5/LPDDR5X memory controllers, and an integrated Arm Mali™-G78AE GPU.

The Versal Prime Series Gen 2 builds upon 40 years of AMD experience in embedded markets, including those with high-security, high-reliability, long-lifecycle, and safety critical applications. Versal Prime Series Gen 2 adaptive SoCs are designed to meet SIL 3 operating requirements and are compliant with numerous other safety and security standards.

HIGHLIGHTS

UP TO 10X SCALAR COMPUTE[1] FOR COMPLEX WORKLOADS

- Over 200k DMIPs of compute with up to 8x Arm Cortex®-A78AE processors
- Expanded caches – 1 MB L3 cache per two-core cluster and 4 MB shared LLC
- Up to 10x Arm Cortex-R52 real-time processors; L1 cache, TCM, 2 MB OCM
- Heterogeneous processing: High-performance scalar compute combined with programmable logic in a single device

SUPERIOR INTEGRATION FOR SYSTEM EFFICIENCY

- New hard video encode & decode – HEVC & AVC up to 4K60, 4:4:4, 12-bit[2]
- DDR5/LPDDR5X memory controllers and updated programmable I/O
- 100G multirate Ethernet and PCIe® Gen5 hard IP
- Integrated 4-core Arm Mali-G78AE GPU for real-time display/HMI

FOR HIGH-SECURITY, SAFETY-CRITICAL APPLICATIONS

- Up to 100k DMIPs of compute at SIL 3 (random) operation[3]
- SIL 3 (random) operation from processing system to NoC to DDR memory
- New application security unit and DDR inline crypto for run-time security
- Secure boot and device configuration through platform management controller

KEY APPLICATIONS

PRO AV AND BROADCAST

UHD Streaming and Recording

Production Switchers

Mobile Wireless Video

AEROSPACE AND DEFENSE

Avionics, UAS, UAM

Image Fusion, Displays

SDR and Networking

INDUSTRIAL AND SMART CITY

Collaborative Robots

Industrial PCs

Factory Automation Cameras

HEALTHCARE

Ultrasound

Endoscopy

3D Imaging

FEATURES

FEATURE	HIGHLIGHTS
Processing System (PS) of Integrated CPUs	• Up to 8x Arm Cortex-A78AE application processors – up to 200k DMIPs • Up to 10x Arm Cortex-R52 real-time processors • Support for USB 3.2, DisplayPort™ 1.4, 10G Ethernet, PCIe® Gen5, and more
Programmable Logic (PL)	• Low-latency, deterministic, parallel processing • Fully customizable to enable differentiated, proprietary algorithms • Field-upgradeable: Adaptable to changing conditions and evolving workloads
Functional Safety	• SIL 3 (random) operation from PS through NoC to DDR memory • Up to 100k DMIPs of compute at SIL 3 (random) operating levels[3] • Entire device designed to SC3 for systematic faults
Security	• New application security unit provides run-time HSM security • Platform management controller manages secure boot and device-level services • DDR memory controllers support inline encryption (AES-XTS or AES-GCM)
Video Codec Unit (VCU)	• Each VCU tile offers hardened encoding & decoding • Support for HEVC & AVC up to 4K60, 4:4:4, 12-bit[2] • Up to two VCU tiles per device; aggregate both tiles for limited 8k30 support
Integrated GPU	• 4-core Arm Mali-G78AE GPU with up to 268 GFLOPs of compute (FP32 MACs)[4] • Four shader cores in 2 slices – configurable as 1 or 2 independent partitions • Support for: OpenGL® ES 3.2, OpenGL SC 2.0, Vulkan® 1.2, Vulkan SC, OpenCL™ 3.0
DDR5/LPDDR5X Memory Controllers	• Support for DDR5 @ 6400 Mb/s and LPDDR5X @ 8533 Mb/s • Up to 170 GB/s memory bandwidth in the largest devices[5] • Flexible pin planning – swap hard controller pins to support other interfaces
Programmable I/O	• New high-performance X5IO support DDR5/LPDDR5X, LVDS, and other standards • New MIPI C-PHY support (4.5 GS/s) to complement 4.5 Gb/s D-PHY support • HDIO and MIO support lower speeds and logic levels up to 3.3V
Network on Chip (NoC)	• High-bandwidth software-programmable network on chip • Data movement alternative to PL-based routing • Assured quality of service (QoS) to prioritize critical traffic
32G High-Speed Serial Transceivers	• Production-proven 32G GTYP transceivers • Up to 20 PL-facing transceivers per device • 4 additional PS-facing transceivers per device for PS-based 10 GbE, PCIe Gen5
100G Multirate Ethernet	• Channelized for 1x100 GbE, 2x50 GbE, 1x40 GbE, 4x25 GbE, or 4x10 GbE • Integrated FECs for robust error correction (KR FEC, KR4 FEC, KP4 FEC) • FEC bypass mode for custom use
PCIe Gen 5	• PL-based support for PCIe Gen5x4, Gen4x8, and other configurations • Hardened PCIe controller IP blocks integrated into programmable logic • Up to 4 PL-based controllers per device; additional PCIe Gen5 controllers in PS

NEXT STEPS

For more information on AMD Versal Prime Series Gen 2, visit **www.amd.com/versal-prime-gen2**

ENDNOTES

1. Based on AMD internal pre-silicon performance estimates for combined total DMIPs of the Versal AI Edge Series Gen 2 and Versal Prime Series Gen 2 processing system when configured with 8 Arm Cortex-A78AE applications cores @2.2 GHz and 10 Arm Cortex-R52 real-time cores @1.05 GHz, compared to the published combined total DMIPs of the processing system in the first-generation Versal AI Edge Series and Versal Prime Series. Versal AI Edge Series Gen 2 and Prime Series Gen 2 operating conditions: Highest available speed grade, 0.88V PS operating voltage, split-mode operation, maximum supported operating frequency. First-generation Versal AI Edge Series and Prime Series operating conditions: Highest available speed grade, 0.88V PS operating voltage, maximum supported operating frequency. Actual DMIPs performance will vary when final products are released in market. (VER-027)
2. Video codec acceleration (including at least the HEVC (H.265), H.264, VP9, and AV1 codecs) is subject to and not operable without inclusion/installation of compatible media players. (GD-176)
3. Based on AMD internal pre-silicon functional safety targets and performance estimates for total DMIPs of the application processing unit (APU) in the Versal AI Edge Series Gen 2 and Versal Prime Series Gen 2 processing system when configured with 8 Arm Cortex-A78AE applications cores @2.2 GHz. Operating conditions: Highest available speed grade, 0.88V PS operating voltage, and maximum supported operating frequency, with all APU cores operating in lock-step mode. Actual performance will vary when final products are released in market. (VER-028)
4. Based on Arm published product specifications for the Versal AI Edge Series Gen 2 and the Versal Prime Series Gen 2 configured with a 4 core Arm Mali-G78AE GPU, maximum operating frequency 1050 MHz, 64 FP32 per ops/clock/core, and 4 texels per ops/clock/core. Actual Versal AI Edge Series Gen 2 and Prime Series Gen 2 product performance will vary when final products are released in market. (VER-030)
5. Based on AMD engineering pre-silicon performance estimates for the Versal AI Edge Series Gen 2 2VE3858 device with 5x 32B memory controllers and expected maximum LPDDR5X memory data rate of 8.533 GB/s, compared to an in-production first-generation Versal AI Edge Series VE2802 device with 3x 64b memory controllers operating at the published maximum LPDDR4X memory bandwidth of 102.4 GB/s. Actual memory bandwidth calculations for the Versal AI Edge Series Gen 2 devices are subject to change when final products are released in market. (VER-031)

DISCLAIMERS

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